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Nanostructuring of free-standing, dielectric membranes using electron-beam lithography

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Nanostructured dielectric membranes are used in several applications ranging from de Broglie matter-wave optical elements to photonic crystals. Precise pattern transfer and high aspect ratio structures are crucial for many applications. The authors present an improved method for direct patterning on free-standing, dielectric membranes using electron-beam (e-beam) lithography. The method is based on an advanced etchmask that both reduces charging and allows for tuning of the etch mask thickness to support high aspect ratios even for small structures. The authors etched structures as small as 50 nm radius holes in a 150 nm thick membrane and achieved aspect ratios of up to 1.3 for this structure size range. The etch mask thickness can be tuned to achieve the required aspect ratio. The etchmask is composed of a three layer stack consisting of poly(methyl methacrylate), SiO_2 and an antireflective coating polymer. Scanning-electron micrographs of membranes produced with the fabrication method are presented. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4820019]

I. INTRODUCTION

Periodic micro- and nanostructured free-standing dielectric membranes exhibit properties useful in a range of applications. Highly sensitive and compact fiber optic pressure and temperature sensors have been demonstrated using photonic crystal silicon based membranes exploiting submicrometer structures in near infrared (IR).[1,2] Dielectric membranes with sub-500 nm periodicity have been made to demonstrate biosensors that potentially can provide sensitivities down to a single molecule.[3,4] Furthermore, dielectric membranes have been structured into free-standing optical (diffraction) elements such as gratings, zone plates, and a Poisson spot annular aperture for the manipulation of de Broglie matter-waves.[5–9]

Optical sensors based on photonic crystal dielectric membranes exploit photonic band gaps[10] and guided resonance modes[11] to achieve sensitivity. These optical properties start to appear when the pattern period is on the order of the operating wavelength. Techniques that facilitate fabrication of structures with periods and features sizes down to 500 nm are hence sufficient for sensors using IR light, i.e., they can be made using standard photolithography techniques. Moreover, IR sensors can be fabricated directly in silicon since it is virtually lossless and can be regarded as a dielectric material for wavelengths longer than 1 μm. Optical sensors operating in the visible range can usually not be made using such fabrication techniques. They typically require pattern periods smaller than 500 nm and the use of dielectric materials such as silicon nitride (Si_3N_4) and silicon dioxide (SiO_2). De Broglie matter-wave optical elements also normally require patterning on a length-scale below what is possible with standard photolithography. The smallest free-standing features made so far for such applications are around 50 nm,[7] and even less would be desirable.[12] This calls for alternative approaches, such as UV or deep UV lithography, electron-beam (e-beam) lithography, nanoimprint lithography, or scanning probe lithography.

In this paper, we will focus on fabricating photonic crystals using maskless e-beam lithography. In order to realize structures using e-beam, an electron sensitive resist is used as the pattern transferring agent. One of the most widespread resists used is the synthetic polymer poly(methyl methacrylate) (PMMA), mainly due to the high achievable patterning resolution.[13]

Using an e-beam for patterning resists on dielectric materials has the potential drawback that dielectric materials generally are insulating. This can cause charge build up, which may deflect the electron beam, resulting in patterning defects and drift in periodic patterns, limiting the minimum feature size.[14] This is especially the case when performing e-beam directly on thin, free-standing dielectric membranes. Charging effects can be reduced by performing lithography while the membrane material is still attached to a conducting or semiconducting substrate.[4] However, this leads to

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complicated fabrication procedures requiring the pattern to be protected from being altered when the conducting substrate is being removed.

After patterning and developing the resist, the pattern is normally transferred to the membrane material through an etch step. This is commonly done using a dry etch, often performed with a reactive ion etcher (RIE). Chemical wet etching is also possible, but dry etch is often preferred for several reasons: With RIE, fragile membranes can be etched with reduced risk of breaking, since the sample does not have to be submerged or lifted out of a chemical etchant. Also a much higher degree of etching anisotropy is normally achieved, resulting in high aspect ratio structures and good pattern definition. Dielectric materials, used in applications for visible light, are most often Si_3N_4 and SiO_2. These two materials have been used in the semiconductor industry for decades and can now be made with an outstanding degree of purity and virtually zero optical loss. It is a problem that, however, reactive ion etching in recipes used to etch these dielectrics also etches PMMA quite aggressively.[15] Consequently, since small features require the use of a thin resist layer to minimize scattering of electrons in the resist,[16] the aspect ratio achievable in dielectrics, using e-beam and only PMMA as a mask is limited for small feature structures. The transferred pattern definition also degrades with increasing aspect ratio since the PMMA pattern tends to taper due to the etch characteristic of the PMMA.[17] Here we present an improved process for direct patterning of free-standing dielectric membranes with e-beam, which reduces charging effects (thus improving the pattern definition) and offers the possibility of high aspect ratios of the membrane structures.

II. FABRICATION TECHNIQUE

The main idea behind the new process is to use a more advanced etch mask. Instead of only transferring the pattern by a single layer of PMMA, we use a very thin layer of chrome on top of the PMMA, a SiO_2 layer, and a layer of antireflective coating (ARC) (Brewer Science XHRIC-11). The bottom layer of ARC is used since as a cross-linked polymer after baking, it has a higher dry etch resistance. That said, using other polymers as etch mask, for example, PMMA is possible, but for the relatively long dry etch times in CF_4 gas ARC has proven superior for the pattern transfer. The mask layers are deposited on the membrane, prior to e-beam exposure, and the simplicity of patterning directly onto the membrane is kept. During exposure, the chrome works as a conducting layer, reducing charge build up at the surface, while PMMA is exposed by electrons traveling through the chrome. The pattern is thus transferred to the SiO_2-layer, which works as a hard etch mask in the following ARC dry etch. We are then left with structured ARC on top of the membrane. Despite the fact that the ARC etches at approximately the same rate as the membrane material in the final step, high aspect ratio patterns can hence be transferred into the membrane in the following anisotropic dry etch. It should be noted that in spite of the name, the ARC is not used for any antireflective purposes in this application, but solely as a polymer etch mask for the pattern transfer into the membrane. The thickness of the PMMA resist can still be kept at a minimum for the patterning, while the ARC thickness can be chosen according to the required membrane etch depth. See Fig. 1 for an overview of the fabrication process. We point out that trilayer/multilayer masks have been used in different variations such as PMMA/germanium/PMMA.[18] In such a mask, the germanium layer serves as the hard etch mask and at the same time prevents charging. This is simpler than our method, which requires an extra step for the chrome. The combination chrome/SiO_2 as conductive layer and hard etch mask is however still a good choice for our application compared with a single intermediate metal layer. Chrome is a superior conductor compared to, for example, germanium, and the electron beam is nearly unaffected by the thin chrome layer. Acquiring a good contact between the sample holder and the thin sandwiched germanium layer might prove challenging. Also the SiO_2 hard etch mask reduces the amount of backscattered electrons, and hence the proximity effect, compared to a metal layer or more dense material.[19] This allows for a better pattern definition, which is an advantage, in particular for small structures.

The substrates used in the fabrication process were free-standing membranes ($900\,\mu m \times 900\,\mu m$) consisting of a $Si_3N_4/SiO_2/Si_3N_4$ thin film stack, where each layer was 50 nm, respectively. The layers were made using standard semiconductor and lithography techniques: The thin-films were deposited in consecutive steps on both sides of a double side polished 200 μm thick 4 in $\langle 100 \rangle$ silicon wafer (n-phosphorus doped with resistivity 1500 Ω cm, made by Topsil). The Si_3N_4 was made by low pressure chemical vapor deposition (LPCVD), and the SiO_2 was made by LPCVD poly-Si deposition followed by thermal oxidation (Fig. 1, step 1). A photolithography step was performed on one side of the wafer, in order to pattern membrane windows on the thin film stack. Then, a dry etch was preformed, using a Plasmatherm 790+ RIE, in order to open the dielectric stack, using 20 SCCM CF4 gas at 600 W and 10 mTorr, which leaves windows of exposed Si on one side of the Si-wafer masked by the dielectric stack (Fig. 1, step 2). Finally, a tetraethylammonium hydroxide (TMAH) wet etch of the wafer silicon was performed. This was done using a 25% TMAH solution at 80 °C, resulting in an etch rate of 22 μm/h. The sample was etched for 10 h, resulting in free-standing membranes supported by a wafer thick silicon frame (Fig. 1, step 3). (If the wafer is exposed to air for more than a couple of minutes after dry etching the mask in the dielectric thin film stack, the wafer should be left in buffer-HF for about 10 s in order to remove any native oxide before proceeding with the TMAH-etch.)

Next, the etch-mask was applied: A 150 nm spin-coated layer of ARC baked at 150 °C for 90 s, 20 nm SiO_2 deposited at a rate of 3 nm/s by electron beam evaporation (EBE), and a 150 nm spin-coated layer of PMMA baked at 175 °C for 3 min (Allresist AR-P 671). To overcome sample charging while patterning, an additional 3 nm chrome layer was deposited on top of the PMMA as a conductive layer using

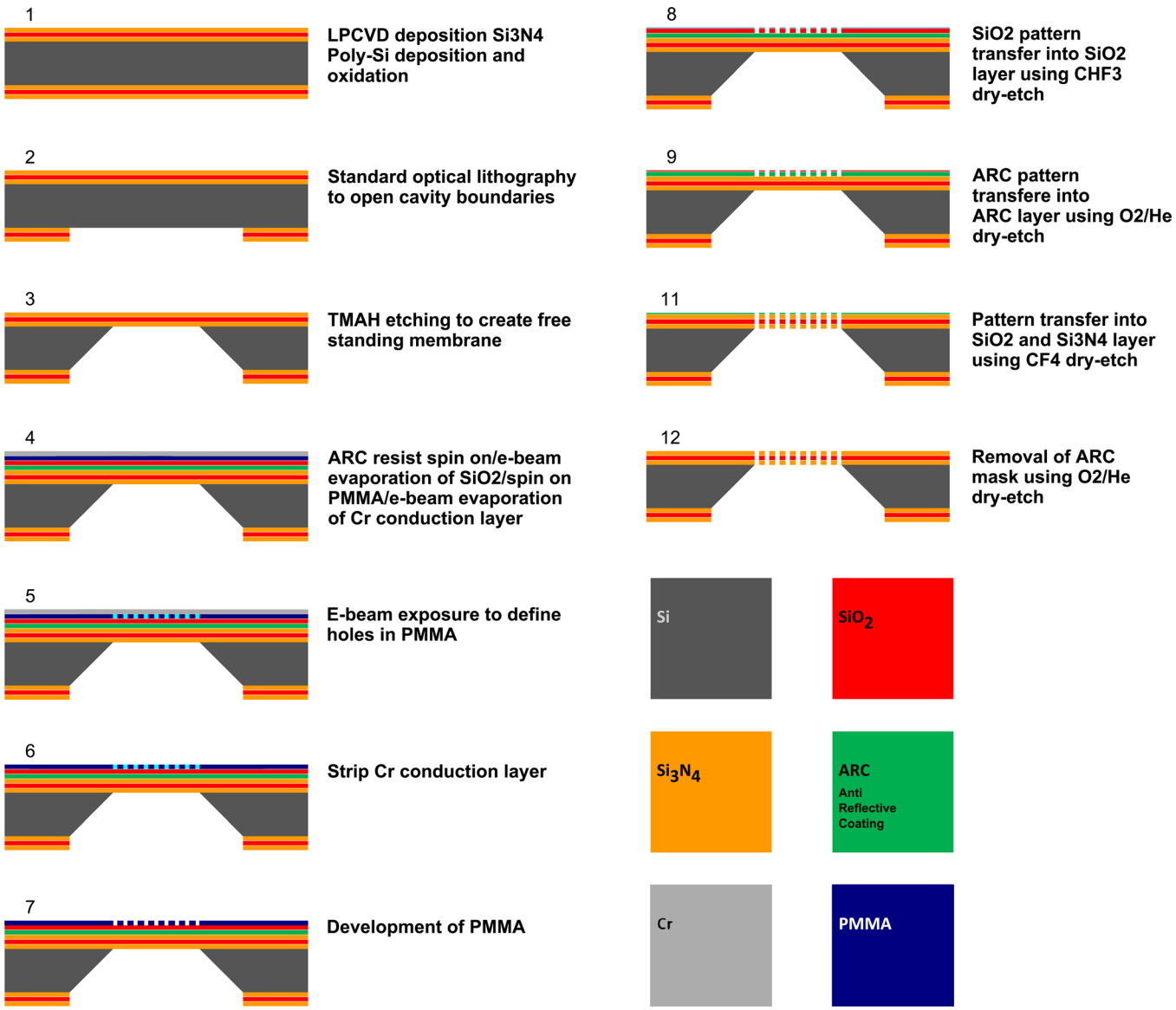
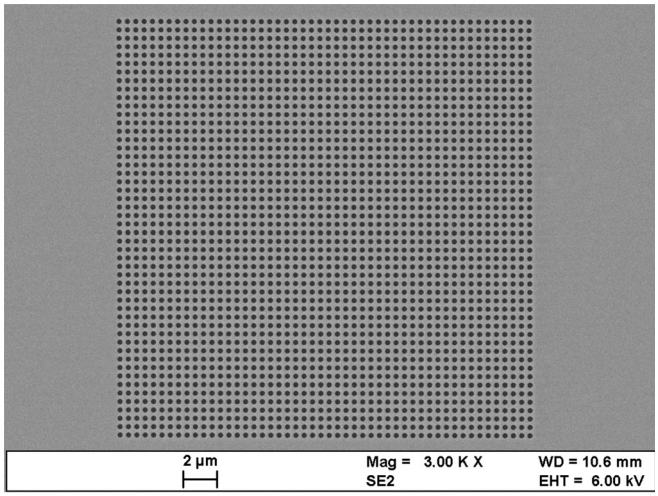


FIG. 1. (Color online) Step by step illustration of the fabrication process. Note that in step 11 the ARC layer is also partially removed, and step 12 removes the remaining ARC.

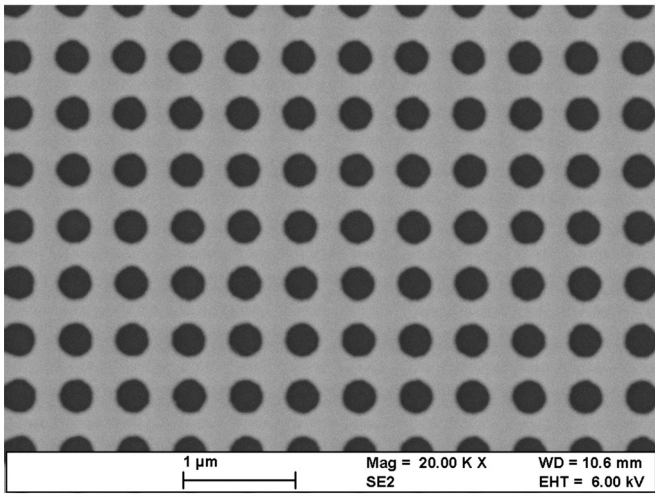
EBE (Fig. 1, step 4). It was found that chrome is a better choice than for example aluminum, since the aluminum-etchant (Transene Company INC. Aluminum Etchant Type A) was seen to etch the PMMA and consequently distort the pattern.

The pattern was exposed with an acceleration voltage of 30 kV and a beam current of 300 pA with a patterning dose of 400 μC/cm^2 (Fig. 1, step 5). These parameters were found to give the optimum shape representation of the designed pattern in the PMMA. With this dose, the resulting hole pattern had dimensions slightly larger than the digitally designed pattern. By means of "shape-biasing," the over-sizing was circumvented by measuring the hole dimensions of a test sample and decreasing the digital pattern design relative to the measured over-sizing.

After e-beam exposure, the chrome was removed using a chrome etchant (Transene Company Inc., Chromium Etchant 1020) for 8 s at 20 (C °C. The etch rate was estimated by coating a glass slide simultaneously with the membranes so both substrates would have the exact same chrome thickness. The glass slide was submerged in the chrome etchant and timed until the glass became colorless and hence the chrome fully removed. By this method, the etch rate was determined to be about 0.8 nm/s. To ensure there were no chrome residues left, we deliberately over-etched the substrates slightly. This could be done since the chrome etchant does not affect the PMMA. Then, the PMMA was developed in an e-beam developer (Allresist GMBH, AR 600-56) for 120 seconds, exposing the underlying SiO2. The SiO2 was dry etched in a 15 SCCM flow of CHF3 gas for 3 min and 30 seconds at a pressure of 7 mTorr and RF power of 100 W. This pattern transfer is needed since the PMMA cannot withstand the subsequent ARC etch. Using the SiO_2 as an etch mask, the pattern was transferred to the ARC using a 10 SCCM He and 5 SCCM O_2 gas flow mix for 10 min at 10 mTorr and 100 W. This also removed most of the PMMA (see Fig. 1 step 8).



(a)



(b)

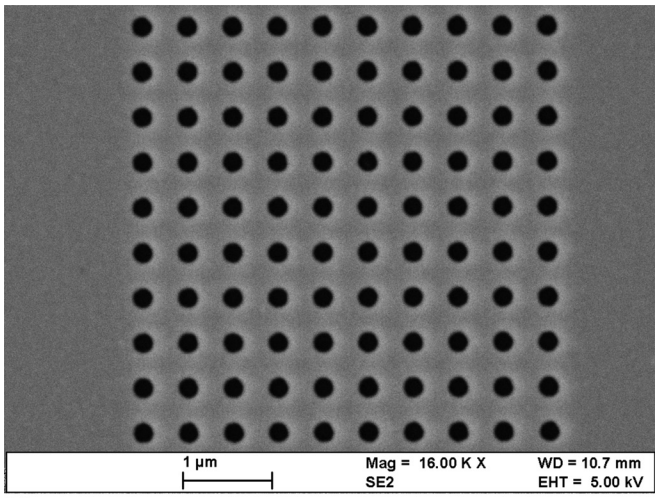
FIG. 2. SEM micrograph of (a) nanostructured dielectric membrane fabricated using the process summarized in Fig. 1, and (b) a close-up of the holes. The lattice is square with a period of 500 nm ± 3 nm. Holes have a radius of 150 nm ± 4 nm.

Finally, the pattern was transferred into the $Si_3N_4/SiO_2/Si_3N_4$ membrane, using a dry etch with 15 SCCM CF_4 gas for 14.5 min at 10 mTorr and 100 W. This etch also removed the SiO_2 mask and the ARC. We determined the etch rate to be about 9 nm/min for the membrane materials, and ~10 nm/min for the ARC, by investigation of a cleaved cross-section using a scanning electron microscope (SEM). The ARC etch rate was hard to determine solely by SEM due to low contrast between the two layers. When the membrane etch is completed, the ARC is also removed. To ensure that all ARC was removed from the membrane, a final ARC etch step was preformed using the same parameters as for the ARC etch above (see Fig. 1, steps 6–12). For stability reasons, the membranes were not etched completely through. 20 nm were left in the bottom of the holes. This is not important for the optical measurements that the membrane samples will be used for.

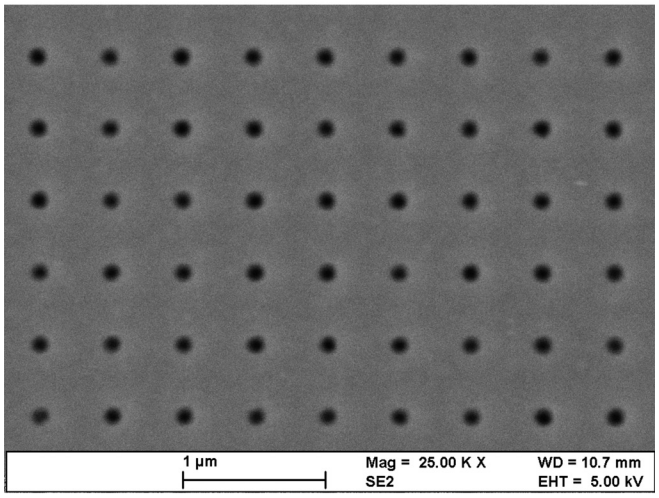
III. RESULTS AND DISCUSSION

Figure 2(a) shows an overview SEM micrograph of a 50 × 50 hole nanostructured dielectric membrane (photonic crystal). We fabricated photonic crystals with three different hole radii 50±6, 100±4, and 150±4 nm shown in Figs. 2(b), 3(a) and 3(b), respectively, all with a period of 500±3 nm. Closeup images can be seen in Figs. 2(b), 3(a) and 3(b). It can clearly be seen that the method works well, even down to the smallest holes with a radius of only 50 nm. The final structures reveal well shaped holes, free from defects and with borderline edge definition.

Figure 4 shows a cross-section SEM image of a sample, fabricated the same way as the photonic crystals, but not on a free-standing membrane. This allowed us to cleave the samples and verify the etch depth into the membrane material. It was measured to be, as expected, 130 nm for the specific ARC thickness used in this experiment. In case of the smallest holes, we can hence estimate that the maximum aspect ratio is as high as 1.3. In order to etch the remaining 20 nm of the membrane, which can be seen in Fig. 4, we could have used a thicker layer of ARC. This would allow even higher aspect ratios to be achieved. However, since the



(a)



(b)

FIG. 3. SEM micrographs of holes with a radius of (a) 100 ± 4 nm and (b) 50 ± 6 nm etched in a 150 nm thick dielectric membrane. Both lattices are square with a period of 500 ± 3 nm.

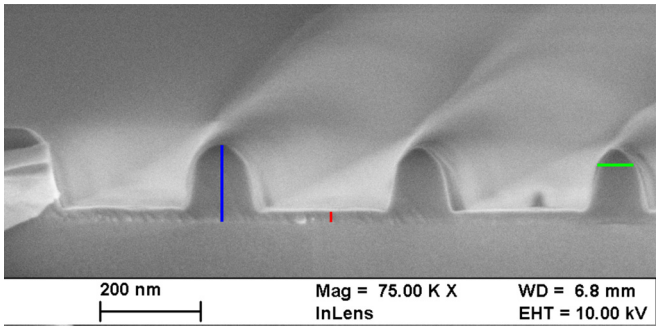


FIG. 4. (Color online) Cleaved test sample imaged at 90° to show the etch profile of the Si_3N_4/ SiO_2/ Si_3N_4 layer. The etched lines are about 250 nm wide, with walls approximately 70 nm in thickness (horizontal bar). The right most vertical bar shows the full thickness of the membrane (150 nm), and the central vertical bar shows the remaining membrane after the etch (20 nm). Calculated aspect ratio for the walls is thus (150-20)/70 ≈ 1.9.

current fabricated structures were used in an optical measurement where this was inconsequential, and a thin layer at the bottom only renders the membrane more mechanically stable, we did not try to increase the etch depth. In Fig. 4, the top of the membrane structures shows sign of rounding. This is caused due to the ARC being spent prematurely so that no mask was present in the last part of the etch. The rounding can be avoided by a thicker ARC layer or shorter etch times.

IV. CONCLUSION

We have developed a new etch mask especially useful for direct patterning, and subsequent dry-etching, of free-standing dielectric membranes using e-beam lithography. The etch mask separate the exposure and development of the resist, from the membrane dry-etch step, thus enabling higher aspect ratios and smaller feature sizes to be patterned. Also a chrome layer is deposited on top of the stack to address the issue of sample charging commonly seen when patterning dielectric membranes. The ARC thickness can be tuned to achieve the required aspect ratio in final devices. SEM micrographs of our fabricated structures shows that the process performs well, when patterning holes, with a radius of down to 50 nm and an aspect ratio of 1.3, directly on free-standing dielectric membranes.

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